A Novel Approach To Dual Damascene Patterning

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Abstract

In this paper, we present and discuss a novel approach to dual damascene patterning based on the invention of SLAM (Sacrificial Light Absorbing Material) [1,2]. We will focus on dual damascene patterning problems that led to the invention of SLAM, and present a side-by-side comparison of the patterning performance of SLAM-assisted dual damascene patterning and a Bottom Anti-Reflective Coating (BARC), the industry's primary approach. SLAM-assisted dual damascene patterning is an enabling technology for Intel's 130nm technology and beyond.

I. Introduction

The adoption of dual damascene copper metalization posed many challenges to the patterning process. Unacceptable variations in substrate reflectivity inhibited the well-controlled patterning of line and space on glass-like interlayer dielectric (ILD). Use of antireflective coating material to suppress substrate reflectivity is a common practice in the industry. However, applying this technique to dual damascene patterning resulted in several defect problems [3,4]. During interconnect line etch, BARC residues and polymer formation resulting from differences in etch selectivity between the BARC and ILD material generates serious defect problems. In spite of recent advancement in organic antireflective coating [4,5], the integrated litho-etch performance is still problematic. Control of substrate reflectivity, the ability to achieve a manufacturable etch process capable of selectively etching the ILD with respect to the etch stop layer (ESL), and the elimination of via shell defect, were strong drivers behind the invention and development of SLAM-assisted dual damascene patterning technology. SLAM is a material that fills the vias and covers the surface of the wafer to provide an opaque and *hole-free* substrate at trench lithography. For example, in a via-first dual damascene integration scheme photoresist will partially fill the vias in an uncontrolled fashion during the trench spin / expose / develop (SED) process. Applying SLAM before the SED process step provides a hole-free substrate eliminating the problem of resist-filled vias. The absorbing nature of SLAM suppresses substrate reflectivity variations and enables controlled printing of line and space structures on glass-like ILD.

II. Material and Process Considerations

The SLAM material was synthesized by adding dye to a member of the siloxane-based family of polymers. The dye exhibits strong absorption characteristics at the desired lithographic exposure wavelength (e.g. 248nm). The absorption characteristic of the SLAM is mainly determined by its dye content. A valid SLAM material must exhibit (a) superior gap fill capability to enable filling of small vias, (b) strong absorption at the exposure wavelength, (c) comparable dry etch and highly selective wet etch performance with respect to the ILD, and (d) compatible with photoresist processing. Through intensive collaboration with Intel's key photoresist and chemical suppliers, we were able to synthesize a SLAM material that meets the above-mentioned criteria.

To reduce the negative impact on the effective dielectric constant of an interconnect system; the thickness of the ESL used in a dual damascene integration scheme is minimized. Etch selectivity between the ILD and ESL during via and trench etch steps dictates the minimum ESL thickness. The introduction of SLAM enabled us to eliminate the dry etch selectivity requirement during trench etch step, since the ESL is not exposed during this step. This facilitated the relaxation of selectivity during the via etch step, and allowed for less constraints on the trench etch process, resulting in optimized profiles and trench depth uniformity.

Another key advantage to SLAM is the fact that a typical oxide etch chemistry can be tuned to achieve equivalent ILD and SLAM etch rates during trench etch step. This particular characteristic of the SLAM eliminated the formation of the via shells and was central to the superior defect and yield performance, compared to other industry approaches.

III. Integration Scheme and Fab Processing

We will focus on dual damascene integration using a via-first scheme without embedded ESL. The ILD system under consideration is fluorosilicate glass (FSG). (dielectric constant is measured to be 3.6) with silicon nitride ESL [6]. The SLAM-assisted dual damascene patterning process, schematically illustrated in Fig.1, was developed for use on Intel's 130nm technology [6,7,8].

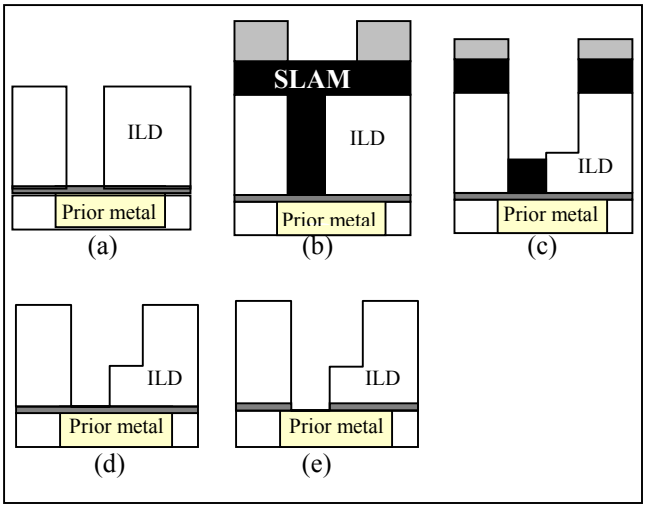


Figure 1: SLAM-assisted dual damascene process flow

There are six layers of interconnects for which the layer pitch, thickness, and aspect ratio are listed in Table 1. Except for the first metal layer, all other layers were patterned using dual damascene technique. The ESL thickness budget is mainly dedicated to the via etch process consumption. To limit the ESL thickness, ILD:ESL etch selectivity of 15-20:1 is needed during the via etch. Achieving such selectivity is difficult, but attainable. Without SLAM presence during the trench etch, the selectivity requirement during via and trench etch becomes impractical.

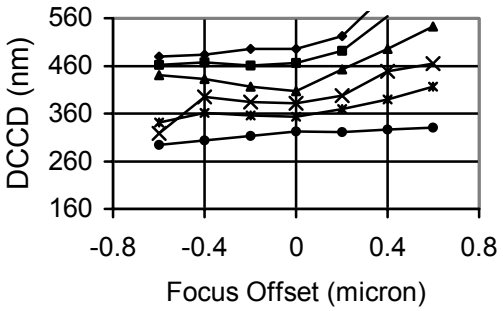
Table 1: Interconnects layers structure [6].

LAYER	PITCH	THICKNESS	AR
Metal 1	293	280	1.7
Metal 2,3	425	360	1.7
Metal 4	718	570	1.6
Metal 5	1064	900	1.7
Metal 6	1143	1200	2.1

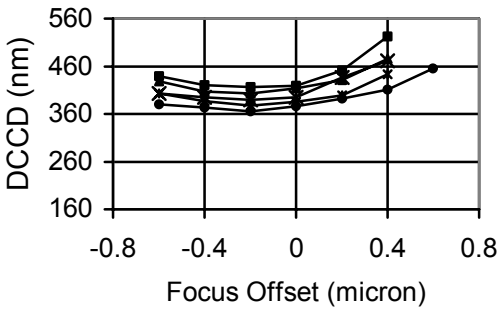
Lithography for via and line/space were performed using 0.60-0.68NA/248nm scanning technology. Feature dimensions are consistent with 130nm technology [7,8]. Both via and trench etch steps were carried out in a parallel plate, magnetically enhanced, RF etch system using CFx / oxygen chemistry. The via etch process was optimized for selectivity to the ESL without degrading via profile. After via etch and cleans are performed (Fig.1a), the wafer is coated with SLAM and patterned with trench photoresist (Fig.1b). Post trench etch, SLAM remains at the bottom of vias and on top of the wafer surface, as illustrated in Fig.1c. SLAM is removed from everywhere on the wafer with high selectivity to the ILD during the post trench etch clean step. The ESL breakthrough step is then performed to expose the underlying copper layer.

III. Results and Discussion

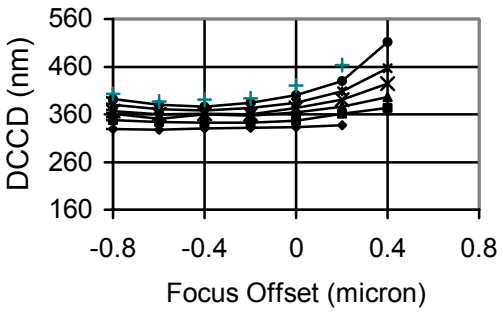
Side-by-side performance comparison between SLAM and BARC –assisted dual damascene was conducted. The trench etch process and cleans were modified, where necessary, for best performance. We start by examining the lithographic performance of the SLAM and BARC materials. The exposure-focus curves for an FSG substrate are given in Fig.2a, and for SLAM and BARC-coated FSG substrates in Fig.2b and Fig.2c, respectively. Those curves represent the sensitivity of critical dimension at develop check step (DCCD) to focus offset at various exposure dose conditions. Exposure dose ranging from 20-40mJ was used.



(a) FSG substrate without reflectivity control.



(b) SLAM-coated FSG substrate.



(c) BARC-coated FSG substrate.

Figure 2: Exposure focus curves for (a) FSG substrate, (b) SLAM-coated FSG, and (c) BARC-coated FSG.

Each curve in Fig.2 represents one exposure dose. In case of SLAM and BARC, higher dose was needed due to the absorbing nature of the substrate. Comparing the lithographic performance of SLAM and BARC-coated FSG substrate

clearly demonstrates the reflective nature of the ILD. In the absence of any reflectivity control, critical dimensions (CDs) are sensitive to exposure dose. Moreover, light reflection from underlying copper lines cause photo resist line pinching. On the other hand, one readily notes the tight CD distribution when either SLAM or BARC is used.

Although the lithographic performance of both BARC and SLAM materials was comparable, the post-trench clean outcome of the dual damascene patterning process was completely different, as evident in the cross section micrographs given in Fig.3a and Fig.3b for SLAM and BARC assisted dual damascene patterning, respectively. While the BARC-assisted patterning resulted in shell defects, the SLAM-assisted approach provided a defect-free dual damascene structure, as shown in Fig.3a.

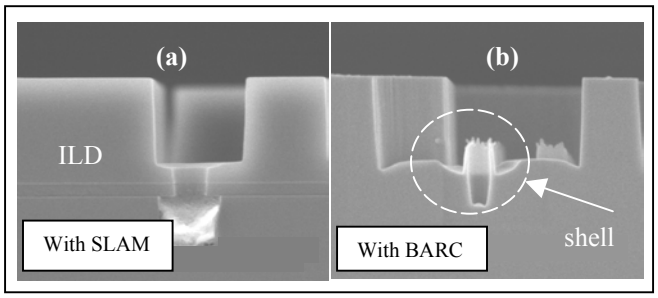


Figure3: Cross section micrograph of dual damascene structures generated using (a) SLAM and (b) BARC.

Shell defect in Fig.3b is composed of a mixture of etch residue, polymer, and ILD. Attempts to remove this defect, either by instituting a dry over etch process or by introducing a post trench etch clean sequence, were unsuccessful.

The overall improvement in profiles and aspect ratios achieved using SLAM-assisted dual damascene patterning can be seen by examining the cross section micrographs of Fig.4, where all six levels of interconnects were built with and without the use of SLAM. In addition to the obvious trench and via profile difference, the absence of SLAM resulted in poor to non-yielding wafers. Poor profiles are the result of the selectivity constraint during via and trench etch. Pre-mature ESL breakthrough and substrate reflectivity effects were significant yield-limiting mechanisms.

IV. Conclusion

The invention and introduction of SLAM provided Intel with an innovative and manufacturable solution to the three dual damascene patterning problems known to the industry. Using SLAM presented lithography with a "hole-free" absorbing substrate, enabled line and space printing on FSG ILD, eliminated shell defects, and relaxed the selectivity requirements of the ILD etch modules to practical levels attainable using existing equipment technology and chemistry. We were able to maintain better patterning performance and achieve a reduced defect levels, compared to the matured aluminum subtractive technology. SLAM-assisted dual damascene patterning is a key enabler for Intel's 130nm technology and is extendable to future technology generations.

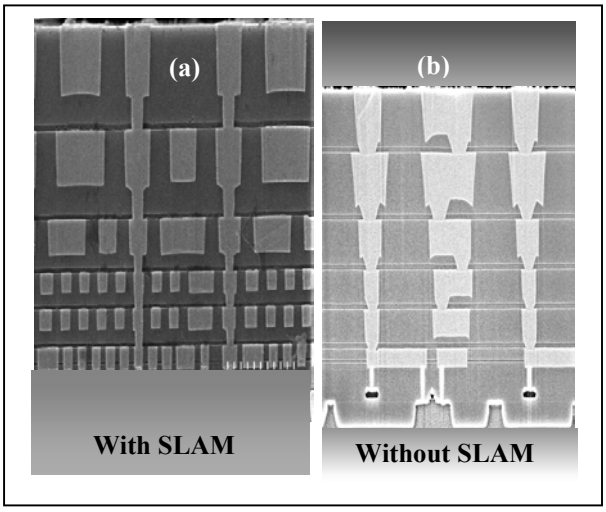


Figure 4: Side-by-side cross section micrograph illustrating the patterning performance of full six levels of interconnect, when SLAM was used (a), and without SLAM in (b).

Acknowledgement

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